

Time Measurement of an Interrupt

An Application Note

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Overview

Developers of drivers and embedded systems often need to measure the elapsed time between events to insure adequate system performance. Typically, these are events that can be detected on the bus such as memory accesses, I/O accesses, and interrupts. American Arium's TRC-xx emulators feature a bus analyzer with a bus cycle time stamp having 10 nanosecond resolution that can be used to measure time between events.

Measuring an Interrupt's Interval

The following example will demonstrate how an American Arium TRC emulator can be utilized to measure the time interval between IRQ0 interrupts. On standard PC platforms, IRQ0 is driven by the equivalent of an 8253 Programmable Interval Timer. This timer divides a 1.19318 MHz signal by 2^{16} , yielding an interrupt every 54.925 milliseconds.

Specifying a Qualifier

The first step in measuring the interval between these IRQ0 interrupts is to specify a qualifier. Qualifiers specify a particular type of bus cycle and determine what is captured in trace. A maximum of two qualifiers may be specified (i.e., Q1 and Q2). Since IRQ0 utilizes an interrupt vector of 08h, we need to specify a single qualifier (Q1) on an interrupt acknowledge of vector 08h as shown in Figure 1.

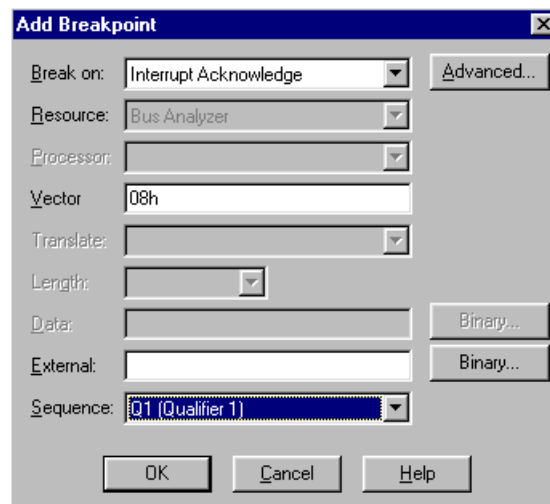


Figure 1: Qualifier 1 (Q1)

Specifying A Qualification Mode To Limit Trace Recording

After defining the qualifier (Q1), the next step to designate how it is to be utilized by specifying the data qualification mode of “record only Q1” as shown in Figure 2. This instructs the bus analyzer to record only the Q1 events previously specified. Keep in mind that regardless of how the bus analyzer records bus activity, it always occurs at full bus speed and never inserts delays of any kind.

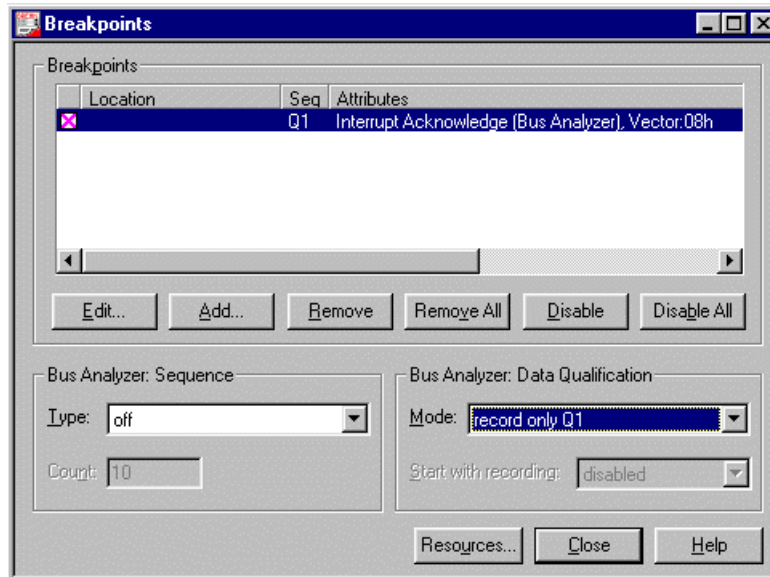


Figure 2: Breakpoints Window

Run, Capture, And View the Interrupt Interval Trace

Finally, we simply need to let the target system run for a few seconds while the bus analyzer captures the Q1 cycles. Figure 3 is a trace window that shows the last seven Q1 cycles that were recorded while the processor was running. Note that in this case, the time stamp on the right side is accumulative and indicates the time elapsed relative to the trigger point (the point at which the processor stopped).

Trace																
STATE	STS	ADDR	DATA	DATA	BE	DID	EXT	STS1	STS2	STS3	STS4	STS5	STS6	TIMESTAMP		
-00007	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	-384.484 ms	
-00006	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	-329.557 ms	
-00005	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	-274.632 ms	
-00004	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	-219.704 ms	
-00003	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	-164.778 ms	
-00002	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	-109.853 ms	
-00001	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	-54.927 ms	
TRIG	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	+0 ns	

Figure 3: Trace Window with an Accumulative Time Stamp

By clicking on the Display Settings button at the bottom of the window, the time stamp can be changed to the delta mode. In delta mode the time stamp indicates the elapsed time between recorded cycles. The time stamp mode can be changed at any time, even after the trace has been captured. Figure 4 shows the same window with the time stamp changed to the delta mode.

Trace

STATE	STS	ADDR	DATA	DATA	BE	DID	EXT	STS1	STS2	STS3	STS4	STS5	STS6	TIMESTAMP	
-00007	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	+54.927 ms
-00006	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	+54.927 ms
-00005	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	+54.926 ms
-00004	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	+54.927 ms
-00003	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	+54.926 ms
-00002	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	+54.926 ms
-00001	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3010	0000	016	+54.926 ms
TRIG	IACK	50000000	-----	-----	08	01	00	0000	41F	110	0000	3210	0000	016	+54.927 ms

-00017

Mixed

Display Settings...

Zero Timestamp

STS Bit Help

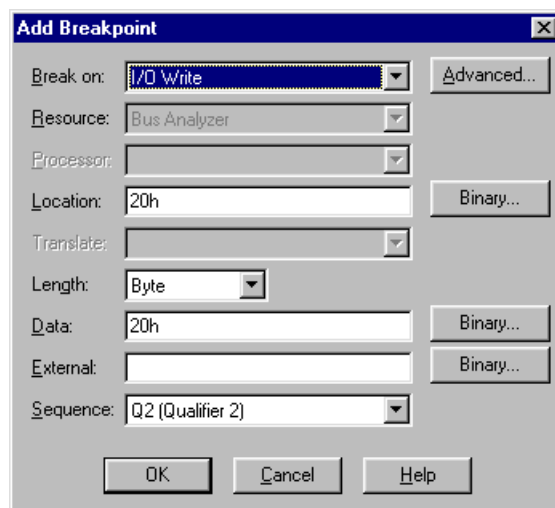
Figure 4: Trace Window with A Delta Time Stamp

Measuring an Interrupt's Duration

In the previous example we measured how often the IRQ0 interrupt occurs. In the next example we will measure the time spent inside the IRQ0 interrupt service routine. We already know that the interrupt starts with an interrupt acknowledge and a little bit of investigation reveals that in this case, it ends with an IRET instruction preceded by a write of 20h to the programmable interrupt controller at I/O port 20h. Therefore, we want to trace from the interrupt acknowledge to the interrupt return instruction and then stop. We will accomplish this by using an additional qualifier (Q2) with a qualification mode of "record on Q1, stop on Q2".

Specifying a Second Qualifier

We will retain the Q1 qualifier from the previous example (Figure 1) which was specified as a vector 08h interrupt acknowledge. Next, we will define a Q2 qualifier that specifies a write of 20h to I/O port 20h as shown in Figure 5. The I/O write to the controller is a better choice than the IRET because the I/O write always appears on the bus while the IRET might become cached and not appear on the bus.



The 'Add Breakpoint' dialog box shows the following settings: Break on: I/O Write, Resource: Bus Analyzer, Processor: (empty), Location: 20h, Translate: (empty), Length: Byte, Data: 20h, External: (empty), Sequence: Q2 (Qualifier 2). There are buttons for 'Advanced...', 'Binary...', 'Binary...', 'Binary...', 'OK', 'Cancel', and 'Help'.

Figure 5: Qualifier 2 (Q2)

Specifying a Breakpoint

Next we will create a breakpoint term to stop the processor on the write to the interrupt controller at I/O port 20h occurs. Terms are similar to qualifiers in that they specify a particular type of bus cycle. They differ from qualifiers in that they are used to stop the processor rather than to control trace recording. Figure 6 shows a Term 1 (T1) bus analyzer breakpoint on this event.

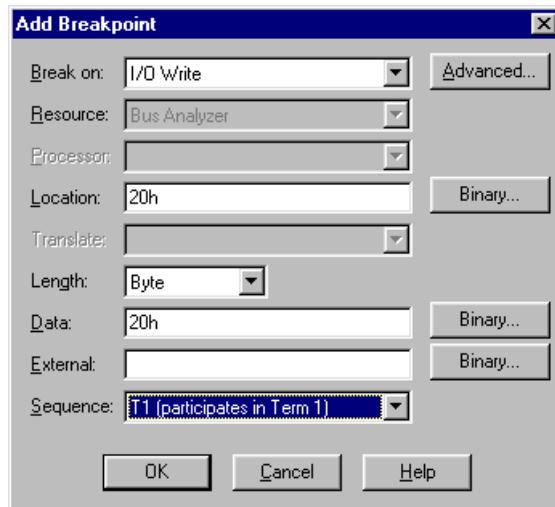


Figure 6: Processor Breakpoint

Specifying a Qualification Mode to Selectively Record Trace

After defining the breakpoint (T1) and both qualifiers (Q1 and Q2), the next step is to designate how the qualifiers are to be utilized by selecting a data qualification mode of “record on Q1, stop on Q2” as shown in Figure 7. This instructs the bus analyzer to begin recording when a match is encountered for the Q1 qualifier and stop recording when a match is encountered for the Q2 qualifier.

We have also specified a bus analyzer sequence of “count of T1” that breaks on the 10th occurrence of the T1 breakpoint. Combined with the qualification mode, this will allow us to capture ten iterations of the interrupt service routine in trace.

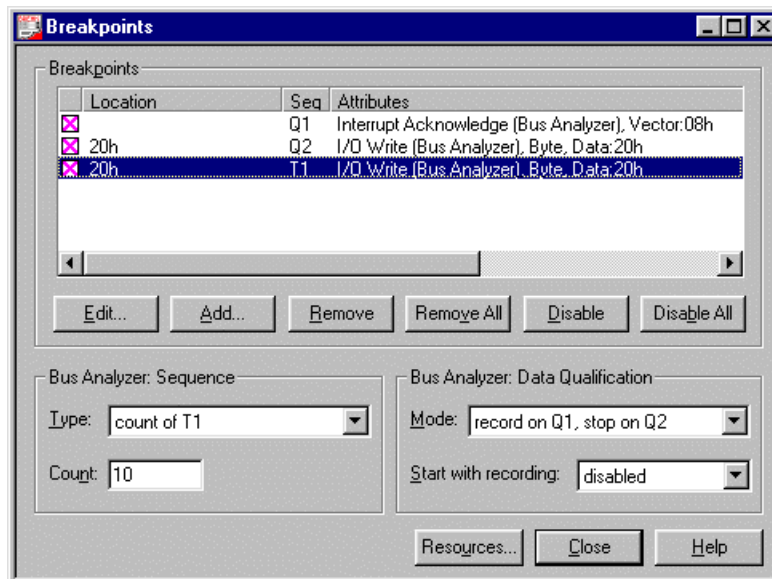


Figure 7: Breakpoints Window

Run, Capture, And View the Interrupt Duration Trace

Finally, we simply need to let the target system run while the bus analyzer repeatedly captures everything that occurs between the Q1 and Q2 qualifiers. Figure 8 is a trace window that shows the last of ten captured iterations of the interrupt service routine. Since the window currently shows the last iteration of the interrupt service routine, you will note that the code is now completely cached and no fetches occurred. As you can easily see, the entire time spent within the service routine was 4.070 μ s.

Trace														
STATE	STS	ADDR	DATA	DATA	BE	DID	EXT	STS1	STS2	STS3	STS4	STS5	STS6	TIMESTAMP
-00013	IACK	50000000	-----	-----08 01 00	0000	41F	110	0000	3010	0000	016			-4.070 us
-00012	BTM	00000000	000EDA2D	000FFEA5 FF 00	0000	49B	110	0000	301C	F400	016			-3.630 us
		000FFEA5	JMP	000FF42CL										
-00011	BTM	00000000	000FFEA8	000FF42C FF 01	0000	49B	110	0000	3214	FF00	016			-3.470 us
		000FF42C	JMP	000FF42EL										
-00010	BTM	00000000	000FF42E	000FF42E FF 00	0000	49B	110	0000	301C	7700	016			-3.300 us
		000FF42E	CALL	00103700L										
-00009	BTM	00000000	000FF431	000F3700 FF 00	0000	49B	110	0000	321C	FE00	016			-3.110 us
		000F3700	RET											
-00008	BTM	00000000	000F3701	000FF431 FF 00	0000	49B	110	0000	301C	F300	016			-2.810 us
		000FF431	STI											
		000FF432	PUSH	DS										
		000FF433	PUSH	AX										
		000FF434	PUSH	DX										
		000FF435	MOV	DS,word ptr CS:[370E]										
		000FF43A	CALL	00103700L										
-00007	BTM	00000000	000FF43D	000F3700 FF 00	0000	49B	110	0000	301C	3E00	016			-2.460 us
		000F3700	RET											
-00006	BTM	00000000	000F3701	000FF43D FF 00	0000	49B	110	0000	301C	FF00	016			-2.160 us
		000FF43D	ADD	word ptr [006C],0001										
		000FF442	ADC	word ptr [006E],0000										
		000FF447	CMP	word ptr [006E],0018										
		000FF44C	JNE	000FF462L										
-00005	BTM	00000000	000FF44E	000FF462 FF 00	0000	49B	110	0000	301C	BF00	016			-1.830 us
		000FF462	CMP	byte ptr [0040],00										
		000FF467	JE	000FF47BL										
-00004	BTM	00000000	000FF469	000FF47B FF 00	0000	49B	110	0000	301C	4100	016			-1.530 us
		000FF47B	INT	1C										
-00003	BTM	00000000	000FF47B	000FFF53 FF 00	0000	49B	110	0000	301C	8600	016			-1.140 us
		000FFF53	IRET											
-00002	BTM	00000000	000FFF54	000FF47D FF 00	0000	49B	110	0000	301C	1200	016			-630 ns
		000FF47D	CLI											
		000FF47E	MOV	AL,20										
		000FF480	OUT	20,AL										
		000FF482	POP	DX										
		000FF483	POP	AX										
		000FF484	POP	DS										
-00001	I/O WR	00000020	-----	-----20 01 00	0000	891	110	0000	B215	220C	016			-390 ns
	TRIG	00000020	-----	-----01 00	0000	88A	110	0000	3015	0000	016			+0 ns

Figure 8: Trace With an Accumulative Time Stamp Showing the Interrupt's Duration



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